Physics 310
Lecture 5b – Transistors

Fri. 2/12	**Ch 8.1-.3:** Transistors	**Lab 4 Notebook**
Mon. 2/15 Wed. 2/17 Thurs. 2/18 Fri. 2/19	**Ch 8.3-.9:** Transistors **Quiz** Ch 8, **Lab 5:** Transistors More of the same **Ch 9, App B-3:** Operational Amplifiers	**Pop take-home Quiz** **HW5**: * ; **Lab 5 Notebook**

For lab: remind them of elements of lab notebook per syllabus. Be careful to do all that is asked and to "sketch" *quantitatively*.

Equipment:
- Lab 5
- Group Problems
- PPT Visuals

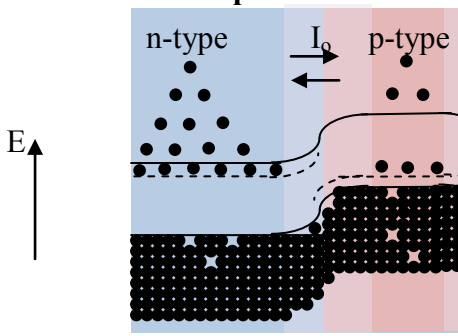
Last time

Ch 8 Transistors

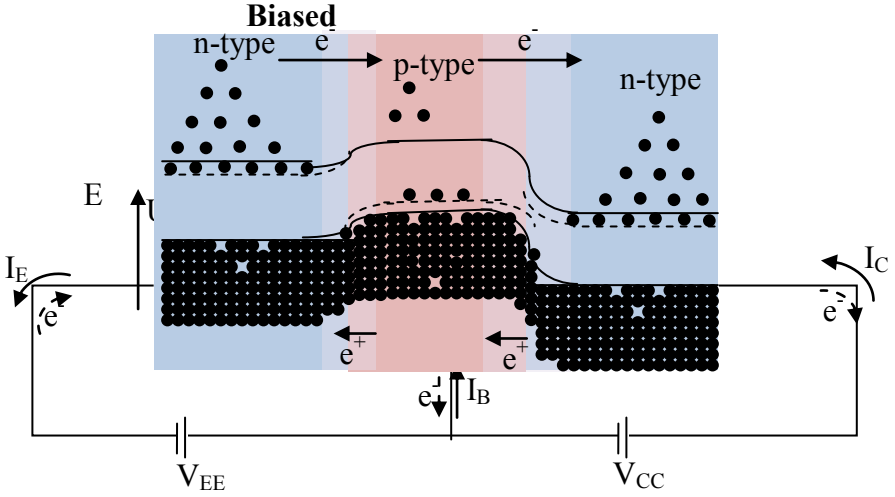
8.1 The Bipolar Junction Transistor

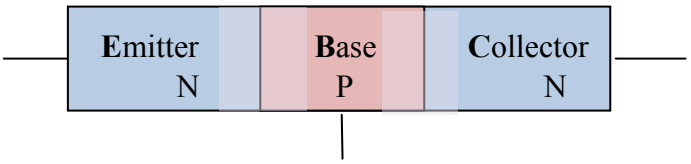
NPN

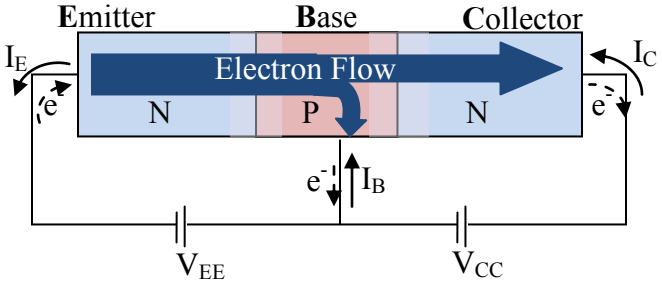
Unpiased

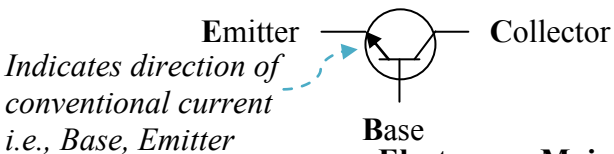


Biased



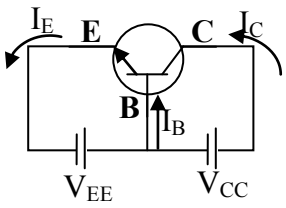






Indicates direction of conventional current i.e., Base, Emitter diode's orientation.

Electrons – Majority Carrier. Base-Barrier.

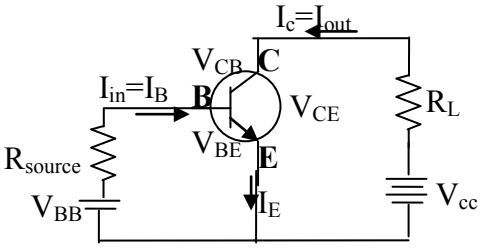


Physics 310
Lecture 5b – Transistors

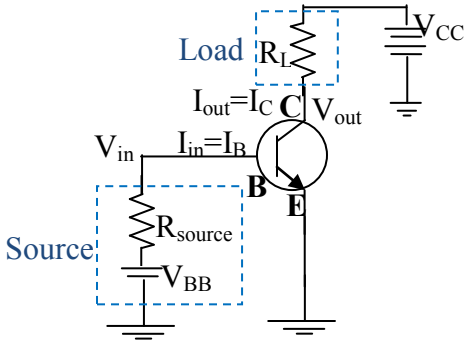
8.1.1 External Circuit Configurations

Common Emitter (emitter wired to common / ground)

The book shows it as



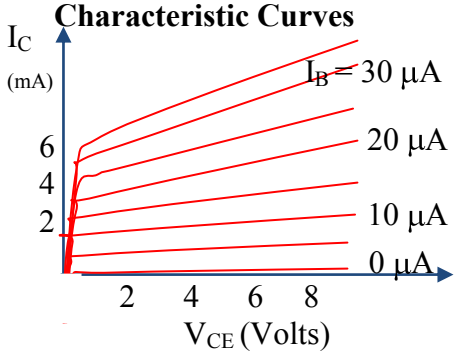
if it helps, we can unwrap it as



Characterizing a Transistor / Convenient definitions

$$V_E = V_B - 0.6\ \text{V} \qquad \beta \equiv \frac{I_C}{I_B} \qquad I_C = I_E - I_B$$

Characteristic Curves

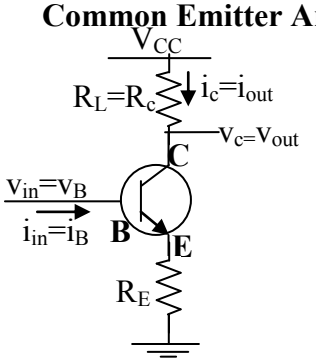


8.2 The Common-Emitter Amplifier

This Time

There are more candidates for being addressed today than we realistically have time for. On the one hand, transistors are at the heart of all devices we'll consider in the remainder of the class; on the other hand, those devices are generally designed so that you don't really need a complete understanding of how the transistors operate to appreciate how the devices function. So, we'll hit on a few things that you're particularly interested in, get a qualitative understanding of FET transistors, and get practice solving some problems with transistors.

Common Emitter Amplifier



Last time we found that the input impedance (that experienced by some device hooked up to the input) is $R_{input} \approx R_E \beta$. We also set up for finding the output impedance (that work is completed in the online notes).

AC Gain. This kind of circuit is usually used to amplify a signal, that is, if there's a small voltage applied at the base, a corresponding large voltage is generated at the collector. The ratio of the two would be the circuit's "voltage gain." In the particular case that you're dealing with just an *AC* signal, or at least that's the only aspect that you're interested in, the *AC Gain* is how the output voltage varies with *variations* in the input voltage.

Target: $Gain_{ACv} \equiv \frac{dv_{out}}{dv_{in}} = \frac{dv_C}{dv_B}$ (this essentially gives the AC voltage gain – neglects any offsets).

Tools: In addition to being able to apply Ohm's law across individual resistors, our basic tools for characterizing the transistor are

$$I_B = I_E - I_C \qquad I_C = \beta I_B \qquad V_E = V_B - 0.6\ \text{V}$$

By applying these rule and Ohm's law, it can be shown (and is within the box below) that

$$Gain_{ACv} = \frac{dv_{out}}{dv_{in}} \approx -\frac{R_C}{R_B}$$

So, let's try to use these relations to phrase the collector voltage as a function of the base voltage and then take the derivative.

$$(v_c - V_{cc}) = -i_c R_c \Rightarrow v_c = V_{cc} - i_c R_c = V_{cc} - \left(i_E \left(\frac{1}{1+\frac{1}{\beta}} \right) \right) R_c = V_{cc} - \left(-\frac{0 - v_E}{R_E} \left(\frac{1}{1+\frac{1}{\beta}} \right) \right) R_c$$

$$v_c = V_{cc} + \left(-\frac{v_B - 0.6V}{R_E} \left(\frac{1}{1+\frac{1}{\beta}} \right) \right) R_c$$

Okay, now we can take the derivative,

$$Gain_{ACv} = \frac{dv_{out}}{dv_{in}} = \frac{dv_C}{dv_B} = -\left(\frac{1}{1+\frac{1}{\beta}} \right) \frac{R_C}{R_B} \approx -\frac{R_C}{R_B}$$

Where the negative sign indicates that the output signal is flipped relative to the input signal.

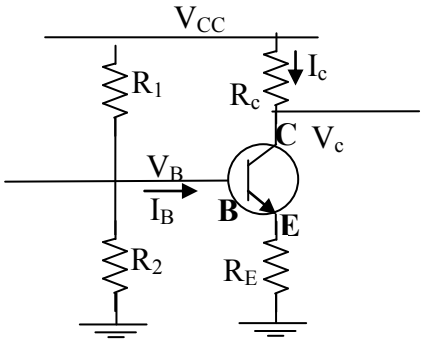
8.2.1 Biasing the Base

"Figure 8.8 has a circuit with four resistors, R1 and R2 aren't used in the process of equations I was wondering how they affect Re. It is fairly similar to problem 1 from the hw**"**

Input Bias. The astute reader might have noticed a problem with this gain. While this may be the voltage gain *while the transistor is functioning properly,* the transistor can't *possibly* produce an output voltage any lower then ground or higher than V_{CC} the way it's wired up.

A related complication is that, as can be seen in the "characteristic curves," β is by no means a constant over the full range; for very small bias currents, the circuit 'turns on' rather dramatically before settling into nice linear behavior.

For both these reasons, it's nice to ensure that V_B is always high enough so that the transistor is "on", even while the input signal itself may oscillate around zero. Thus we modify the circuit just a little to offset the signal presented to the base. The first step in doing this is adding a voltage divider at the input.



We've already calculated the transistor's input impedance, i.e., what single resistor could replace the transistor and yield the same current drawn in the base for the same base voltage, that was

$$R_{input} \approx R_E \beta$$

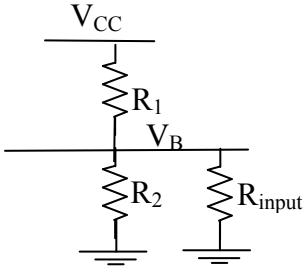
(not quite right for a *DC* signal, but, gets the right ballpark for an argument we'll make.)

So, from the perspective of the base, the circuit looks like a voltage divider

$$V_B = \frac{R_{2-input}}{R_{2-input} + R_1} V_{CC} = \frac{1}{1 + R_1 \frac{1}{R_{2-input}}} V_{CC}$$

Then $\dfrac{1}{1 + R_1 (1/R_2 + 1/R_{input})} V_{CC}$

$\dfrac{1}{1 + R_1 (1/R_2 + 1/(\beta R_E))} V_{CC}$

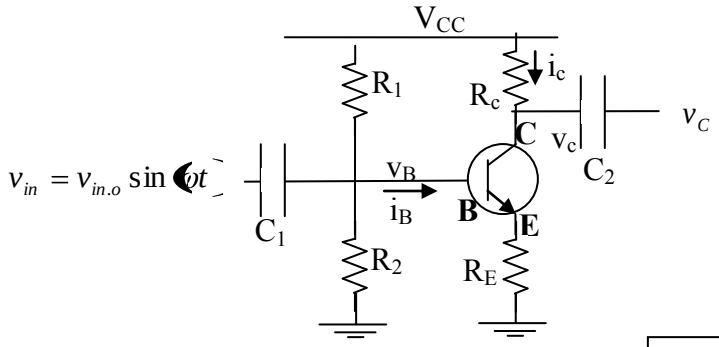


Since the input impedance is quite large (thanks to $\beta >> 1$), for reasonable R_1 and R_2, we have

$$V_{B.bias} \approx \frac{1}{1 + R_1 (1/R_2)} V_{CC} .$$

So, R_1 and R_2 would largely determine the base voltage in the absence of any other input signal. We'll call that $V_{B\,bias}$, and it's the base "bias" voltage.

Now, if we put a capacitor between this voltage divider and an input signal, the circuit looks like



The signal at the base is then

$$V_B \approx V_{B.bias} + v_{in}$$

$$V_B \approx \frac{1}{1+R_1/R_2}V_{CC} + v_{in.o}\sin(\omega t)$$

I haven't verified for myself that this is strictly true, but qualitatively it makes sense – the capacitor and resistors act as a high-pass filter, and don't affect any DC offset so as long as the input signal frequency is high enough, this should be a good approx.

So it mimics the input signal, but rather than oscillating around zero, it oscillates around the bias voltage (you'll notice that a capacitor has also been added to the output so whatever additional bit of circuitry receives this circuit's output can play a similar game and set the voltage bias that *it* wants.) Recall that the transistor circuit can only produce outputs between V_{cc} and ground. So, we want to choose our input bias voltage (by choosing our R_1 and R_2) so the corresponding output bias is right in the middle of this range – that would maximize the range of input signals for which the circuit behaved well.

How do we choose the right resistors?

You can easily work out (see box)

So, we have

$$V_{B.bias} = \left(\frac{1}{R_1/R_2+1}\right)V_{CC}\,.$$

And we want the output biased to be in the middle of the allowed range,

$$V_{C.bias} = \tfrac{1}{2}V_{CC}$$

If we say the transistor has a DC voltage gain of G (that is, $V_C/V_B = G$), then we want the base biased to only

$V_{B.bias} = V_{C.bias}/G$ Putting these two together, $V_{B.bias} = \left(\tfrac{1}{2}V_{CC}\right)/G$

or plugging in our expression for $V_{B.bias}$ in terms of the resistances,

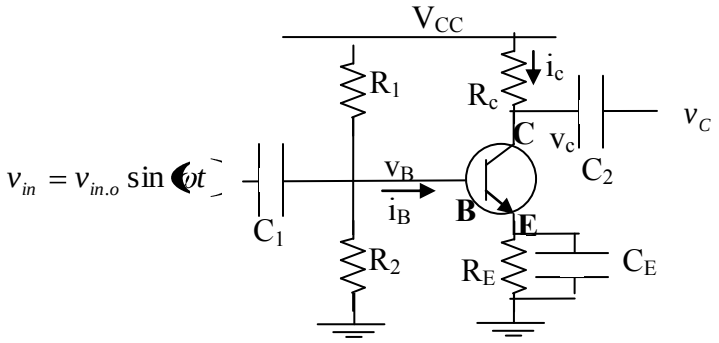
$2G = R_1/R_2 + 1$

or

$R_1/R_2 = 2G - 1$

Thermal Stability

A very high gain circuit operating on an AC signal oscillates between passing a lot of current, and not so much. While in the high-current fraction of its oscillation, the transistor can get it hot. Raising its temperature means increasing the carrier population in the transistor, and thus decreasing its effective resistance and increasing the current still more. Effectively, the circuit's *gain* oscillates – distorting the output signal. This is addressed by putting a capacitor in parallel with the emitter resistor.



This replaces R_E with $\vec{Z}_E = \dfrac{R_E}{1+j(R_E C_E 2\pi f)} = \dfrac{R_E}{\sqrt{1+(R_E C_E 2\pi f)^2}} e^{-j\tan^{-1}(R_E C_E 2\pi f)}$ as the reactance

and the gain is then $G_{ACv} \approx \dfrac{R_C}{\vec{Z}_E} = \dfrac{R_C}{R_E}\sqrt{1+(R_E C_E 2\pi f)^2}\, e^{j\tan^{-1}(R_E C_E 2\pi f)}$

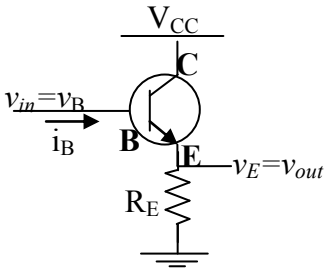
Clearly, the gain increases with frequency; but so does the input impedance, $Z_{in} \approx \beta Z_E$. Now, if we're only planning on running relatively high frequency signals through this, then we can still have a large gain but not necessarily draw as large a current – keeping things cooler and stable.

All told, the common emitter configuration is pretty handy.

"Can you go over what a common collector is and why they are important?"

8.3 Common Collector - Emitter Follower

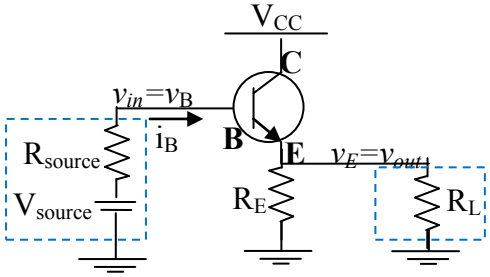
Now let's consider the Common Collector configuration. This can be used as a "follower." Again, calling one of the legs "common" essentially means that it's the one that's *not* got either the input or the output signal.



Now the collector is wired directly to the positive power supply, and we're outputting the emitter voltage. At first blush, you might ask "what's the point?" Since $V_E = V_B - 0.6V$, there's no real *voltage* gain (just a slight DC offset, that doesn't even matter for AC signals); however, there is a *current* gain.

Qualitatively, here's the beauty: the transistor acts as a *buffer* between two chunks of circuitry – (within reason) regardless of how much current is drawn out the emitter, it maintains the same voltage as dictated by the input at the base. So, for example, if you have a voltage divider wired up to the base, then the emitter maintains the desired voltage (dropped by 0.6V) regardless of what it's wired up to!

To quantitatively make this point, we'll imagine wiring this up to some source and some load.



(AC) Input Impedance.

$$R_{in} \equiv \frac{dv_{in}}{di_{in}} = \frac{dv_B}{di_B}$$ (example of circuit algebra, solve for v_b in terms of i_b)

$$v_B = v_E + 0.6V$$

$$0 - v_E = -i_E R_{E-L}$$

$$R_{E-L} = \frac{R_E R_L}{R_E + R_L}$$

$$i_E = i_B(1+\beta)$$

$$v_B = i_B(1+\beta)\frac{R_E R_L}{R_E + R_L} + 0.6V$$

$$R_{in} = \frac{dv_B}{di_B} = (1+\beta)\frac{R_E R_L}{R_E + R_L} \approx \beta \frac{R_E R_L}{R_E + R_L}$$

With $\beta >> 1$, the input impedance can easily be mega-ohms. One implication is that *very little current gets drawn from the source* and across the source's internal resistance; this means that there's very little voltage drop across the source's resistance and so $V_{source} \approx V_B = V_E + 0.6V$, *regardless* (mostly) of R_L.

Output Impedance. (worth citing process and solution, but not working out all details)

$$R_{out} = R_{thev} = \frac{v_{out-open}}{i_{out-short}}$$

$$v_{out-open} = i_E R_E = i_B (1+\beta) R_E = \frac{V_{source} - v_B}{R_{source}} (1+\beta) R_E = \frac{V_{source} - (v_{out-open} + 0.6V)}{R_{source}} (1+\beta) R_E$$

Solving for $v_{out\text{-}open}$ gives

$$v_{out-open} = \frac{\frac{V_{source} - 0.6V}{R_{source}} (1+\beta) R_E}{1 + \frac{R_E}{R_{source}} (1+\beta)}$$

Now, the shorted output current would be

$$i_{out-short} = i_B (1+\beta) = \frac{V_{source} - 0.6V}{R_{Source}} (1+\beta)$$

So,

$$R_{out} = R_{thev} = \frac{v_{out-open}}{i_{out-short}} = \boxed{\frac{R_E}{1 + \frac{R_E}{R_{source}} (1+\beta)} \approx \frac{R_{source}}{\beta}}$$

If $\beta >> 1$, then the output impedance can be quite tiny. That means that a *very big current can be drawn* for the output voltage.

There we have it, there's a very small current draw from the source (large input impedance), but still a lot of current can be supplied at the output (small output impedance.)

Current Gain. With the "input" on the base and the "output" on the Emitter, one could roughly say that the current gain is

$\frac{i_E}{i_B} = \beta$. Of course, some of that current gets siphoned off, through R_E rather than going through the load. *That* current is a fraction of the total current coming out the emitter:

$$i_{Load} = i_E \frac{R_E + R_L}{R_L} \text{ or } i_{Load} = i_B \beta \left(\frac{R_E}{R_L} + 1 \right)$$

In lab you'll construct a follower like that above except the emitter resistor is connected to V_{EE} *not* equal to ground. Then the relation for the output voltage changes to

$$v_{out-open} = i_E R_E + V_{EE} = \frac{V_{source} - (v_{out-open} + 0.6V)}{R_{source}}(+\beta)R_E + V_{EE}$$ so, solving gives

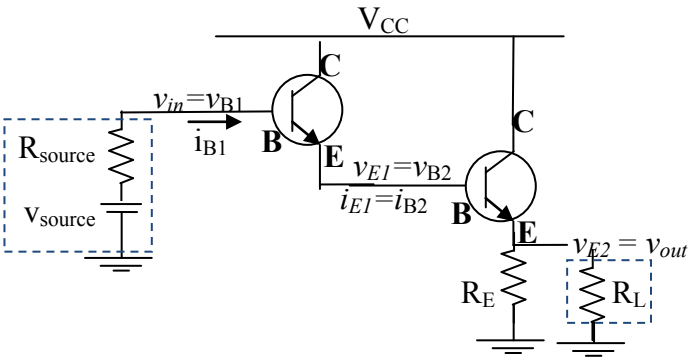
$$v_{out-open} = \frac{(V_{source} - 0.6V)(+\beta)\frac{R_E}{R_{source}} + V_{EE}}{1 + (+\beta)\frac{R_E}{R_{source}}}$$

Now, if b is much greater than 1 (which it should be), then

$$v_{out-open} \approx (V_{source} - 0.6V) + V_{EE}\frac{R_{source}}{\beta R_E}$$

8.4 The Darlington Configuration

What if you want even *more* current gain? You daisy chain two common collector transistor in what's called the "Darlington" configuration.



Current Gain

$$i_{source} = i_{B1} = \frac{1}{\beta_1+1}i_{E1} = \frac{1}{\beta_1+1}i_{B2} = \frac{1}{\beta_1+1}\frac{1}{\beta_2+1}i_{E2} \Rightarrow \frac{i_{E2}}{i_{B1}} = (\beta_1+1)(\beta_2+1) \approx \beta_1\beta_2$$

So the effective β of the combined transistors can be huge!

Strictly speaking, to relate the source current to the load current, we again have to factor in that only a fraction of the current exiting the emitter goes through the load (some goes through R_E.) Thus

$$\frac{i_L}{i_{source}} = (\beta_1+1)(\beta_2+1)\left(\frac{R_E}{R_L}+1\right)$$

Input & Impedance

The Darlington has the same input impedance as does a single common collector transistor.

$$R_{in} = \frac{dv_{B1}}{di_{B1}}$$

$$v_{B1} = v_{E2} + 2*0.6V$$

$$v_{E2} = i_{E2} R_{E-L}$$

$$R_{E-L} = \frac{R_E R_L}{R_E + R_L},\ i_{E2} = i_{B1}(\beta_1 + 1)(\beta_2 + 1)$$

$$v_{E2} = i_{B1}(\beta_1 + 1)(\beta_2 + 1)\frac{R_E R_L}{R_E + R_L}$$

$$v_{B1} = i_{B1}(\beta_1 + 1)(\beta_2 + 1)\frac{R_E R_L}{R_E + R_L} + 2*0.6V$$

$$I_{E2} = i_{B1}(1+\beta_1)(1+\beta_2) \Rightarrow di_B = di_E / (1+\beta_1)(1+\beta_2) \approx di_E / \beta_1\beta_2$$

$$R_{in} = \frac{R_E R_L}{R_E + R_L}(\beta_1 + 1)(\beta_2 + 1)$$

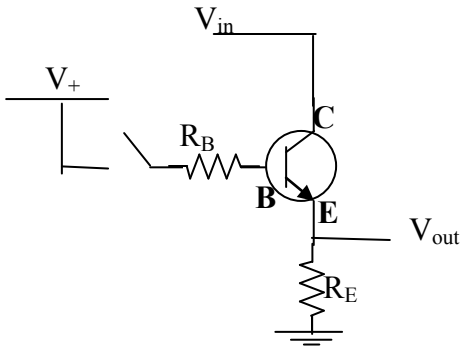
The output impedance can be found to be $R_{out} \equiv \frac{v_{out-open}}{i_{out-short}} \approx \frac{R_{source}}{\beta_1\beta_2}$ via a similar derivation to that for the lone common collector transistor.

(**note**: in the book's equations 8-23 and 8-24, the β^2 should really be $\beta_1\beta_2$)

8.5 The Transistor Switch and Logic

The transistor is the basic unit of integrated circuits that, themselves, are the building blocks of all the electronic components that augment our modern lives. It is comparatively rare for a lone transistor be used; however, there is one rather common application: a transistor switch.

"**Common" *Collector* Switch**



Mechanical Switch Open -> Transistor Switch Open

$V_{out} = 0$ because negligible current flows through R_E, so

$$V_{out} - 0 = i_E R_E \approx 0 \Rightarrow V_{out} \approx 0$$

Mechanical Switch Closed -> Transistor Switch Closed

$$V_{out} - 0 = i_E R_E$$

$$i_E = i_B + i_c = (1+\beta) i_B$$

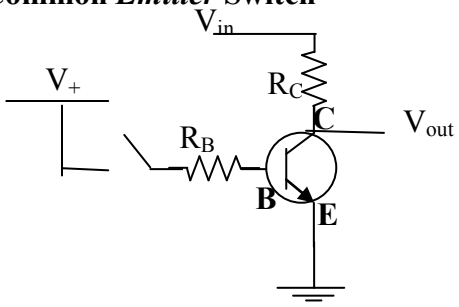
$$i_B = (V_+ - V_{out} - 0.6V) / R_B$$

$$V_{out} = (1+\beta)(V_+ - V_{out} - 0.6V)\frac{R_E}{R_B}$$

$$V_{out} = \frac{(1+\beta)(V_+ - 0.6V)}{1+(1+\beta)\frac{R_E}{R_B}} \approx (V_+ - 0.6V)\frac{R_B}{R_E} \le V_+$$

Which, as long as R_B is a bit more than R_E means that V_{out} hits the ceiling at V_+. Notice that the exact value of V_{in} just doesn't mater (it just needs to be greater than V_B for the transistor to operate properly), so it's usually just wired to V_+.

Common *Emitter* Switch



Mechanical Switch Open -> Transistor Switch Closed

When the mechanical switch is open, there is no base current, so there is only a negligible collector and emitter current. That means that there's no voltage drop across R_C, and thus the output voltage is essentially the input voltage:

$$V_{out} - V_{in} = -i_c R_c \approx 0 \Rightarrow V_{out} \approx V_{in}$$

It's important to point out that *this* switch can actually pass the specific value on V_{in}.

Mechanical Switch Closed -> Transistor Switch Open

When the mechanical switch is closed, then there is a base current and there is a collector current,

$$V_{out} - V_{in} = -i_c R_c$$

$$i_c = \beta i_B$$

$$i_B = \frac{V_+ - 0.6V}{R_B}$$

$$V_{out} = V_{in} - \beta \frac{R_c}{R_B}\left(V_+ - 0.6V\right) \geq 0$$

Or, since the second term is apt to be larger than the first term, and the least V_{out} can really be is 0 (assuming $V_{in}>0$),

$$V_{out} = 0$$

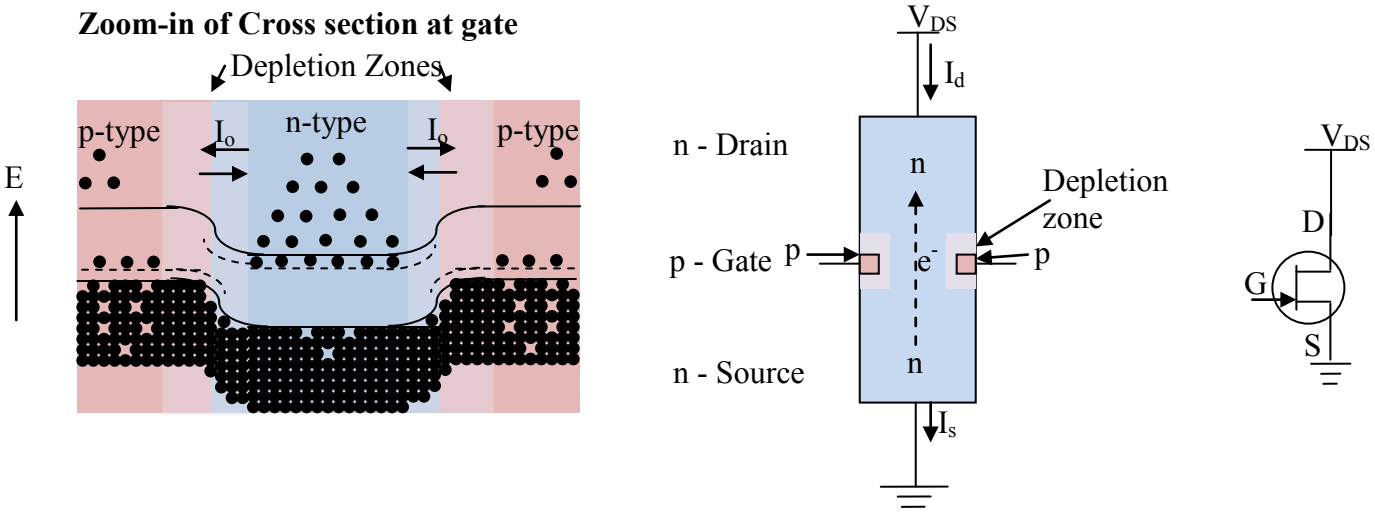
Note: if $V_{in}<0$, then, in principle, the Collector is like an Emitter and the Emitter is like a Collector – it's like we flipped the transistor to have a common – collector switch (though I wouldn't expect it to behave too well since it wasn't designed for that.)

8.6 Junction Field Effect Transistors

- **Transition.** We've spent a lot of time considering transistor circuits built around NPN Bipolar Junction transistors, and very similar circuits can be built of PNP transistors. There is a radically different kind of transistor that's worth knowing about, the Junction Field Effect Transistor, or the J-FET for short.
- **Qualitative Plumbing Analogy.** Qualitatively, to appreciate how the J-FET differs from the bipolar junction transistor, we'll imagine a plumbing analog.
    - **Bipolar Junction Transistor.** Think of the regular Bipolar Junction transistor as a stretch of flexible piping – it has a constant width and bends in it like in the figures on page 2 of the notes. The amount of flow down the length of the device depends on the voltage drops *down stream,* that from the collector to the base, and that from the base on to the emitter. The steeper these drops, the more current flows along the device.
    - **Field Effect Transistor.** In contrast, a J-FET transistor is like a stretch of piping with a collar in the middle; that collar can be choked down or opened up to allow less or more flow. Sure, you still need an over-all voltage drop to drive current, but it's this widening and narrowing of the collar that plays the key role in controlling the flow.

- **Depletion Zone at Junction.** The key to understanding how these J-FET's work is understanding what goes on at the junction. Here are a few different representations of the device.

Unbiased

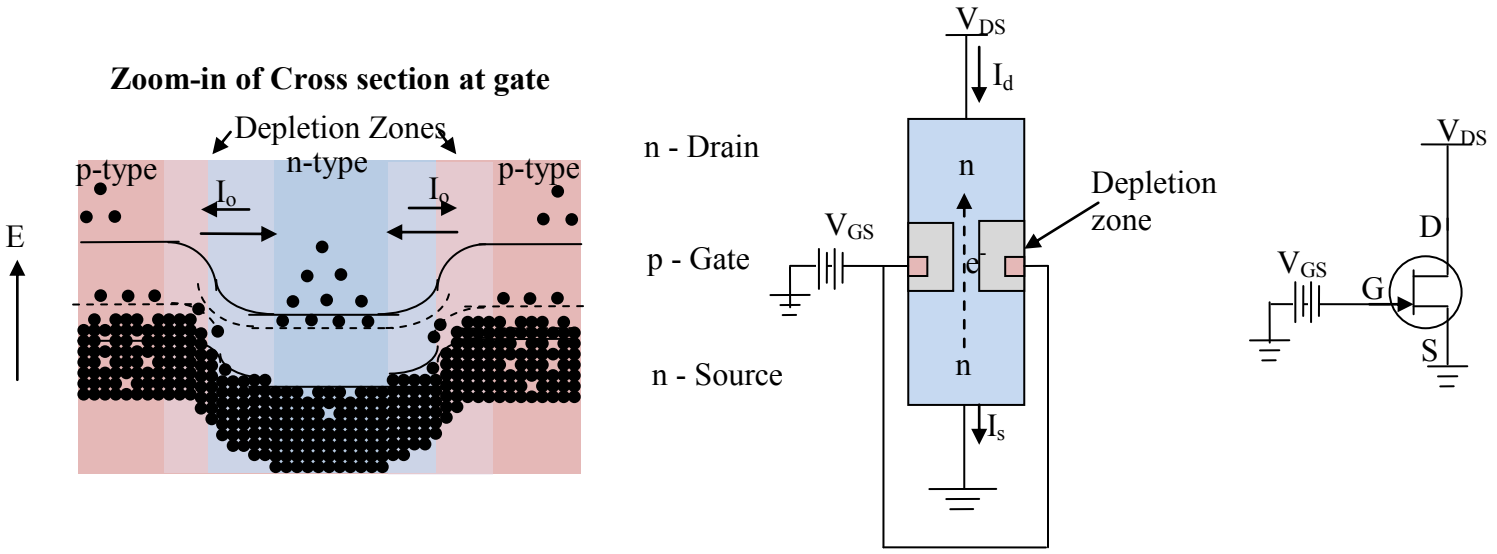


  - **Unbiased.** First we'll look at it in the simple case, with the "gate" disconnected, and refresh our memory on the fundamental physics going on right at the junctions between N and P-type materials (stuff we first considered when we met Diodes last week.) Even when no additional voltage is applied to the P-type material, its energy levels shift relative to those in the N-type. This happens because, right at the junction, the extra electrons of the "donor" atoms in the N-type now have the option of migrating just a *little* over into the P-type and 'falling' down to join "acceptor" atoms. Thus they reduce their energies, and, in the process create a small charge separation (more electrons on the P-side of the junction than on the N-side) and so an electric field and so a voltage and energy difference. This process is self-limiting – the more electrons migrate, the greater the electric field impeding subsequent electrons from doing the same, so eventually an equilibrium is established. That's what's responsible for the bending of the energy levels right at the junctions. This all should make sense and sound familiar from when we met the Diode. Now here's a part that, though true for any N-P junction, wasn't important enough to merit our attention before. Each electron that opts to leave a "donor" and join an "acceptor" is one less electron to get thermally promoted into the conduction band of the N-type (and one less hole to get thermally created in the valence band of the P-type). So, right around the junction, there is a "Depletion Zone" where there aren't so many mobile charge carriers (electrons in the conduction band and holes in the valence band.) With such a low carrier density, the Depletion Zone is a very poor conductor. Looking at the figure below, the wider the Depletion Zone is, the narrower the remaining channel through which current can flow down the transistor from the Drain to the Source.

- **Biased.** The width of the Depletion Zone (and, conversely, the narrowness of the channel) can be increased by biasing the Gate, as illustrated here.

Biased

Zoom-in of Cross section at gate

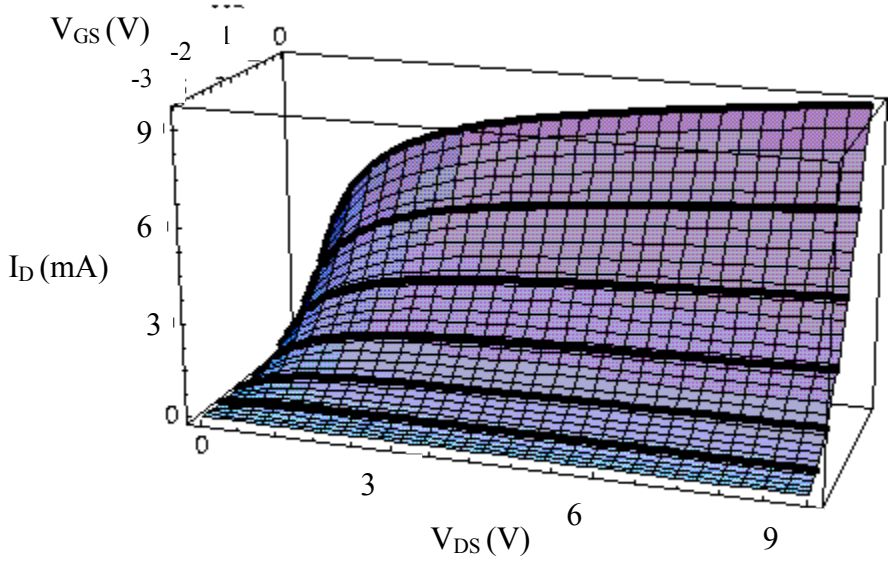


Thus the current flowing from Drain to Source is controlled by the difference between the voltage applied to the gate and that in the channel, which would roughly be the average of the drain voltage and the source voltage: $V_G - \frac{V_D + V_S}{2}$.

Characteristic Curves and Pinch Voltage.

Three variables commonly characterize a JFET's behavior, V_{GS}, V_{DS}, and I_D. Their relation to each other could be plotted in 3D as something like

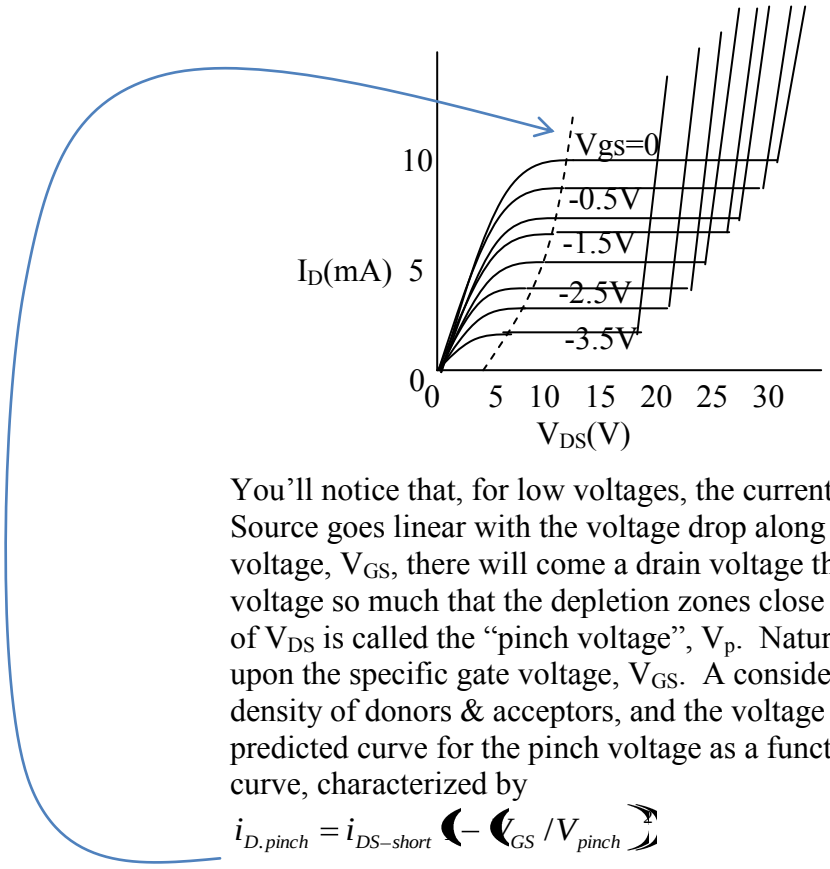
Curtsey of http://www.physics.csbsju.edu/trace/CC.html



Let's call this surface the "Operating Surface." As the JFET operates it's constrained so that its V_{GS}, I_D, and V_{DS} values are on this surface. The dark lines trace curves of constant V_{GS}. These are called "Characteristic Curves."

I_D vs V_{DS} Characteristic Curves

First, looking straight down the V_{GS} axis, and zooming out a little we see this.



You'll notice that, for low voltages, the current flowing down the transistor and out the Source goes linear with the voltage drop along its length, V_{DS}. However, for a given gate voltage, V_{GS}, there will come a drain voltage that corresponds to increasing the channel voltage so much that the depletion zones close in and *pinches-off* the channel. That value of V_{DS} is called the "pinch voltage", V_p. Naturally, the exact V_{DS} that does it depends upon the specific gate voltage, V_{GS}. A consideration of the geometry of the device, the density of donors & acceptors, and the voltage established in a depletion zone leads to a predicted curve for the pinch voltage as a function of the drain current – that's the dashed curve, characterized by

$$i_{D.pinch} = i_{DS-short}\left(1 - V_{GS}/V_{pinch}\right)^2$$

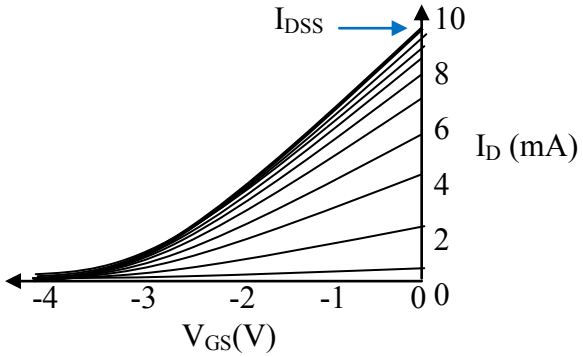
(for a derivation, see section 6-4-1 of P.C. Dunn's Gateway into Electronics)

where $i_{DS\text{-}short}$ is the current that passes in the Drain (and essentially that which passes on out the source) when the gate is short-circuited to the Source (say, both drain and source are grounded).

For higher voltages, the current remains fairly constant, until…something like a Zeener breakdown occurs between the gate and the drain, causing an avalanche of current, and the sudden jump on the right side of the plot.

I_D vs V_{GS} Transfer Curves

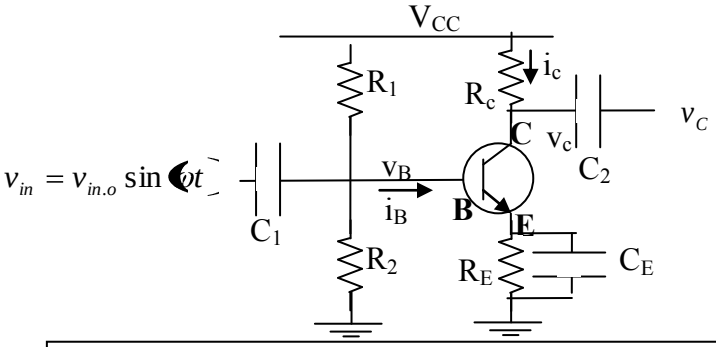
Look back at the 3-D rendering for a moment, see what the constant-V_{DS} curves look like – roughly parabolic. Looking down the VDS axis would look something like this.



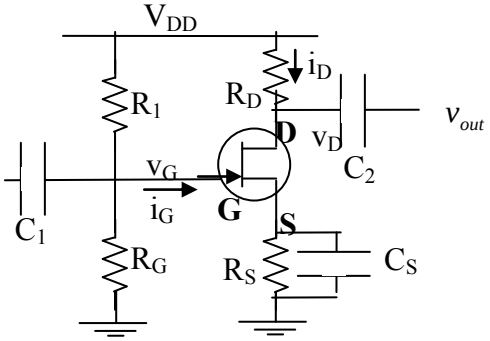
These graphical representations of the relationships between the three parameters, ID, VGS, and VDS, will help us visualize our analysis of a JFET in operation.

8.7 **The FET Amplifier** (for greater discussion, see Ch 6 of J.J. Brophy's Basic Electronics for Scientists.)

Well, now that we've familiarized ourselves with the basic character of a J-FET, let's see it in operation – the FET Amplifier in Common Source configuration. This is the J-FET's take on the Bipolar Junction's Common Emitter set-up that was discussed in section 8.3.



Common *Emitter* with input/output capacitors for AC signal (ignore offset), Base Bias, and Emitter capacitor for high-frequency stability



Common *Source* with same external circuit

Before we set our sites on any particular result, here are a few things worth knowing about a JFET in use.

In principle, $I_D = I_S + I_G$ (since the channel carriers are electrons and the gate carriers are holes out of the device in this configuration, or equivalently electrons into it); however, a J-FET passes very little current between the Gate and the Source-Drain channel, (the sizable depletion zone acts as a barrier; read Section 8.10 about insulated gate transistors / MOSFET's to see this taken to the extreme), so

$$I_G << I_D, I_S$$

thus

$$I_D \approx I_S$$

More specifically, I_D is often in the mA range while I_G is in the nA range. So, even with a very large resistance between the Gate and ground, R_G on order of 0.1 to 10 MΩ, and an even larger resistor links it to the supply line,R_1 around 20 to 100 MΩ.

$$V_G << V_D, V_S$$

Now, generally, when you wire up a transistor, the values of the resistors and the supply voltage (R_1, R_G, R_S, and V_{DD}) are set, i.e., they're constants. Then the variables are I_D, V_G (or V_{GS}) and V_D (or V_{DS}). If you supply an input voltage, then all three of these should be uniquely determined by that input voltage and the three constants (R_1, R_G, R_S, and V_{DD}.) We'll set about relating these variables to each other and the constants for the simplest case – when there is no input. So, we'll be finding the idle, or offset values of these current and voltages.

Operating Point. To visualize what we'll be doing, consider this. In I_D, V_{GS}, V_{DS} space, a JFET's operation 'lives' on the 3D surface illustrated on page 19. At a given moment (with given resistances, supply voltage, and input voltage), the set of values that the JFET has, (I_D, V_{GS}, V_{DS}) define a point on that surface, that is referred to as the "operating point." Here's how we go about nailing down that Operating Point.

Load-Line (in V_{DS} – I_D plane.) Tracing the voltage drop down from V_{DD} to ground (for a DC current, or approximately for a low frequency current), we have

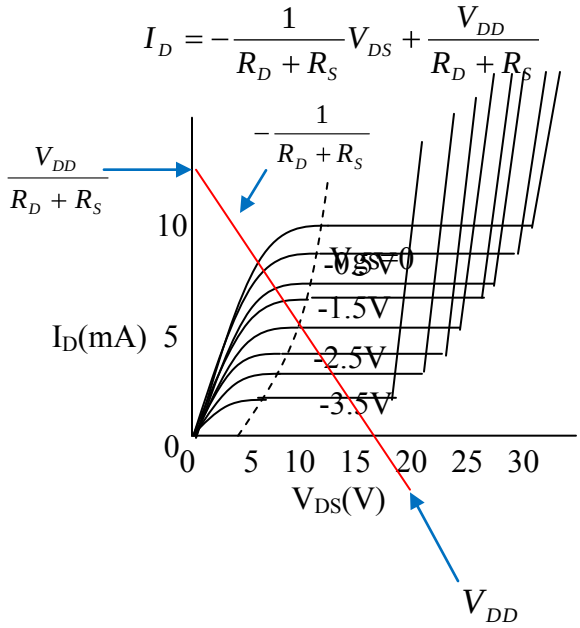
$$(V_{DD} - V_D) = I_D R_D$$

, but $V_D = V_{DS} + I_S R_S$, but if $I_D \approx I_S$,

that's $V_D = V_{DS} + I_D R_S$

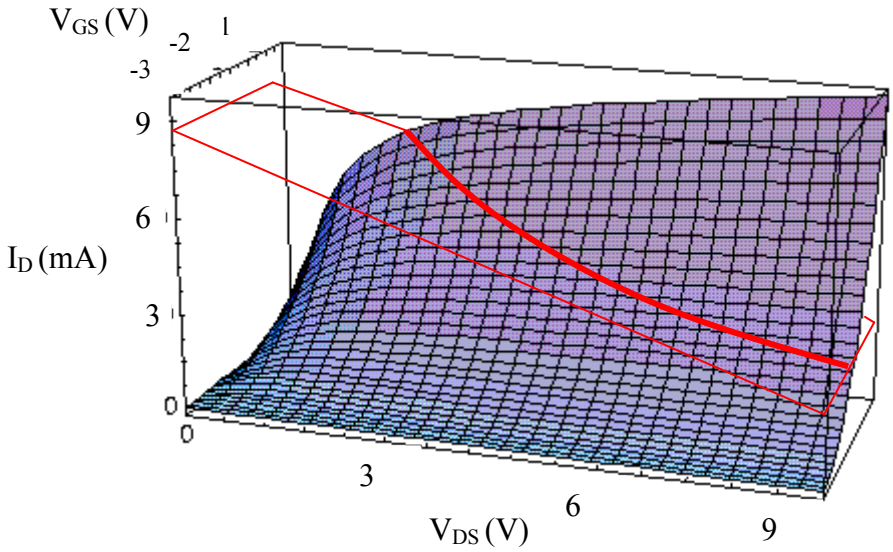
So $$(V_{DD} - V_{DS} - I_D R_S) = I_D R_D \Rightarrow I_D = \frac{V_{DD} - V_{DS}}{R_D + R_S}$$

Re-arranging this a tad casts it as an equation of a line in the V_{ds}-I_d plane, i.e., that in which we've sketched the Characteristic Curves. This is referred to as the "Load Line."



Looked at that way, R_D+R_S set the slope as well as the intercepts of that line.

In the 3D space of ID, VGS, VDS, we have defined a plane that slices through the Operating Surface. Where this plane intersects the surface defines a curve. As the JFET is constrained to both 'live' on this plane and on the Operating surface, it is constrained to live on the curve where they intersect. We're one step closer to nailing down the Operating Point.



Bias Line (in V_{GS} – I_D plane). Now for a little more math.

$$V_{gs} = V_g - V_s$$

Where $V_s = I_s R_s$, but $I_s \approx I_d$ so $V_s = I_d R_s$

As for V_g, assuming that negligible current runs in the gate, compared with that running through R_1 and R_g, then the R_1 and R_g approximately form a voltage divider giving the voltage at the gate as approximately

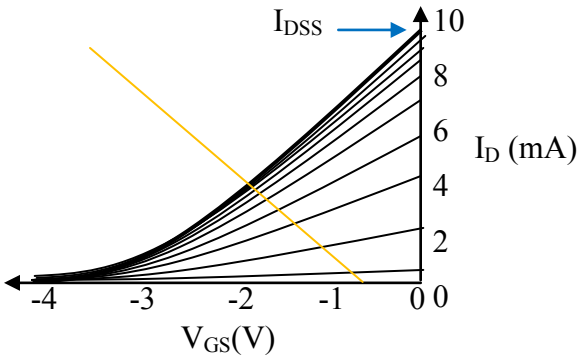
$$V_g \approx V_{dd} \frac{R_g}{R_1 + R_g}$$

Therefore, we have

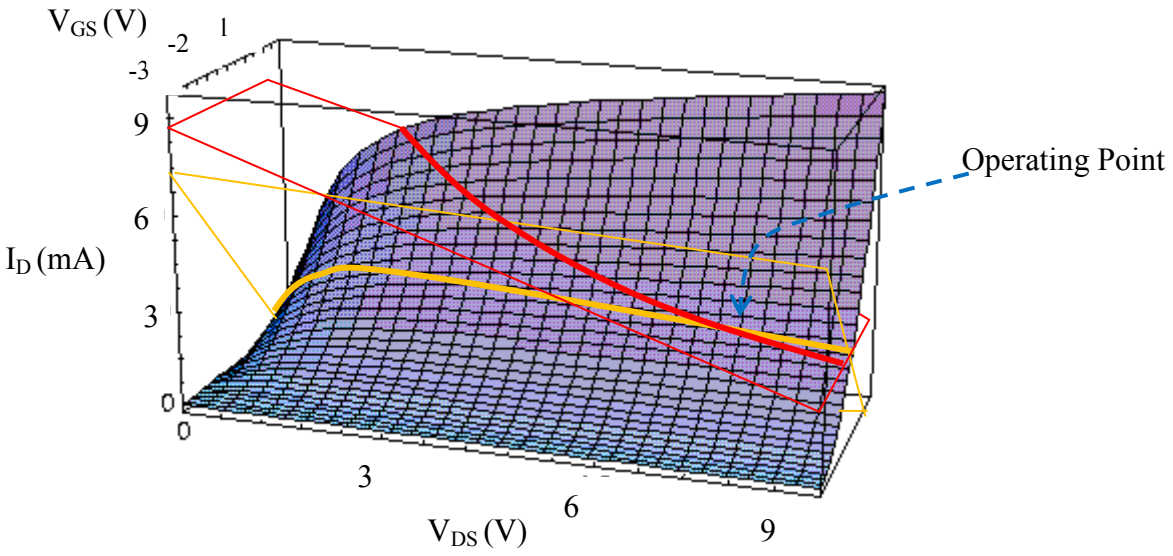
$$V_{gs} = V_{dd} \frac{R_g}{R_1 + R_g} - I_d R_s .$$

Flipping this around to solve for Id, we have another equation of a line, this time in the V_{gs}-I_d plane. It's known as the Bias Line.

$$I_d = -\frac{1}{R_s} V_{gs} + \frac{V_{dd} R_g}{R_1 + R_g \; R_s}$$



In the V_{DS}, V_{GS}, I_D space, it defines a corresponding plane.



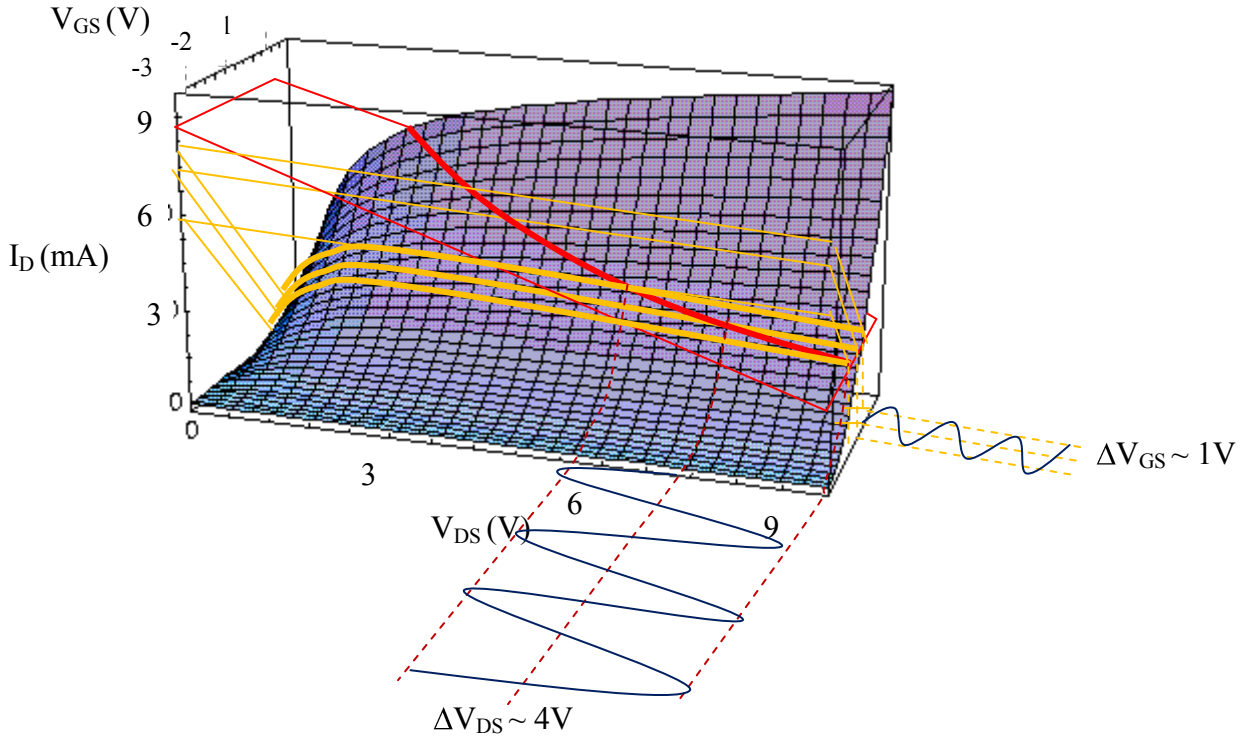
Again, this plane slices through the Operating Surface, and since the JFET's operation is confined to both, it is confined to the curve of their intersection. But since it's also confined to the curve of the intersection of the Load Plane and the Operating Surface, it is completely confined to the point where these two curves intersect – the Operating Point! Thus, Voltages and current are uniquely determined. All this was argues assuming that we had no input signal, so we've got a qualitative sense for how the idle, or offset values of V_{DS}, V_{GS}, and I_D are set. Clearly, there would be a considerable, though steady, output signal even when there is no input signal.

Include Input Signal

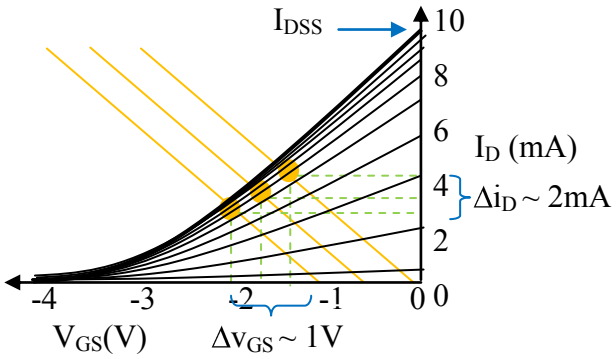
Now, if all you're interested in doing is amplifying an AC signal, you don't care about these offsets. So you put capacitors on the output and input lines. Qualitatively, we can reason how the circuit would process an AC input signal.

Adding an oscilating input signal would wiggle the gate voltage just as if we were varying R1. Looking at the equation of our Bias Line, the effect *that* would have is wiggling the line's offset (while maintaining its slope). In the 3D plot on page 23, that essentially slides the yellow curve up and down the Operating surface, thus changing the point of its intersection with the red line – the operating point.

As illustrated below, an oscillating V_{GS} leads to a larger, *amplified*, oscillating V_{DS}.



From this particular angle, it's a little harder to see, but changing VGS means also changing I_D. Let's say that, viewed in the V_{GS}-I_D plane, the three operating points illustrated here are



The ratio of the *output* variation in current to the *input* variation in voltage is the "Transconductance",

$$g_m \equiv \frac{\Delta i_D}{\Delta v_{gs}}$$

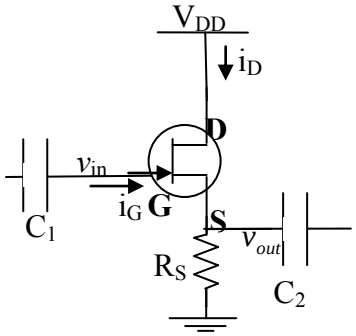
Looking back at the circuit, we can recall that $\frac{V_{DD} - V_D}{R_D} = I_D$ so a variation in the current of Δi_D results in a variation of the drain voltage of $\Delta v_D = -\Delta i_D R_D$.

Then the ratio of variations in the *output voltage* to variations in the *input voltage,* i.e., the voltage gain, is

$$A_v = \frac{\Delta v_D}{\Delta v_{GS}} = R_D g_m .$$

8.8 FET Follower

Now that we've tackled the FET in a slightly complicated circuit, we'll back off and look at one that's as simple as can be.



Let's see how the input and output are related.

$$V_{in} - V_{out} = V_{GS}$$

Now, if we're just concerned with AC signals (as I've suggested by wiring this up through capacitors), then we can recast this as

$$\Delta v_{in} - \Delta v_{out} = \Delta v_{GS}$$

$$\text{where } g_m \equiv \frac{\Delta i_D}{\Delta v_{gs}} \text{ or } \Delta v_{gs} = \frac{\Delta i_D}{g_m}$$

$$\text{but } V_{out} = I_D R_S \text{ so } \Delta i_D = \frac{\Delta v_{out}}{R_S}$$

Putting these together gives

$$\Delta v_{in} - \Delta v_{out} = \frac{\Delta v_{out}}{g_m R_S}$$

or

$$\Delta v_{out} = \frac{\Delta v_{in}}{1 + \frac{1}{g_m R_S}}$$

That's a fairly general result, but, if we have a fairly large R_S, such that $\frac{1}{g_m R_S} << 1$ (and that's quite often the case), then

$$\Delta v_{out} \approx \Delta v_{in}$$

You may ask, 'so what's the point of using a FET like this?' The answer lies in the fact that the FET draws exceedingly little current in its Gate. So this circuit has a very high input impedance. It makes a great follower.