

**Physics 310**  
**Lab 8 – Digital Circuits**

**General Procedures:**

Not all circuits are given, so be sure to sketch all of the circuits that you construct!

When using digital ICs, it is a good practice to put a 0.1  $\mu\text{F}$  tantalum capacitor between the pins connected to the positive power supply and ground. This will reduce problems that might arise if there is some noise in the power supply. Tantalum capacitors are polarized, so be careful about how they are connected.

For this lab, you will be using a digital design board. There are no bus strips along the top or bottom of the breadboard. The following are the features that will be used:

Logic Indicators – A light will be off when its input is LOW and on when its input is HIGH.

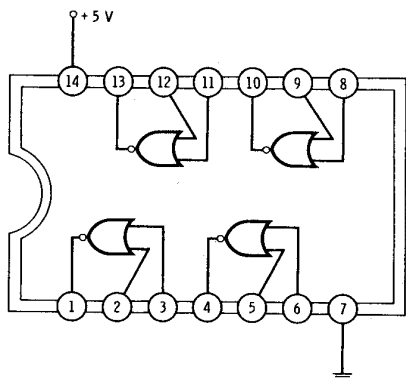
These can be used to test the outputs of gates.

Clock - The CLK output is a square wave with a selectable frequency. The  $\overline{\text{CLK}}$  output is just the inverse of the CLK output.

Logic Switches – The A output is LOW when the switch is set to  $\overline{A}$  and HIGH when the switch is set to A. The  $\overline{A}$  output is the inverse of the A output. The operation of the B switch is similar.

**8-1. NOR gates**

- A. The 7402 is a TTL quadruple 2-input NOR gate with the connections shown below. Make the connections to ground and +5 V. Don't forget the filter capacitor. The truth table for a single NOR gate is also given below.

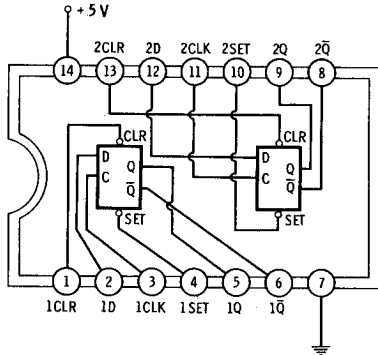


A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

- B. Use the NOR gates on the IC to construct an inverter (NOT gate), an AND gate, an OR gate, and a NAND gate (problem 11-9 from the homework). For each circuit, use the A and B logic switches to vary the inputs and one of the logic indicators to test the output. Draw each circuit and the truth table that you observe for it.
- C. Leave the 7402 on the board with power supply and ground connections for part 8-2.

## 8-2. Data Flip-Flops

- A. The 7474 is a TTL dual data flip-flop with the connections shown below. Make the connections to ground and +5 V. Also, connect the set and clear (CLR) pins to +5 V for normal operation. When set becomes high, the output is set to  $Q=1$  and  $\bar{Q}=0$ . When clear (also called reset) becomes high, the output is reset to the state  $Q=0$  and  $\bar{Q}=1$ . The truth table shows the behavior of a single data flip-flop when set and clear are kept low. It indicates how the levels of the outputs change as the level of the clock input changes. "X" means the input does not matter.

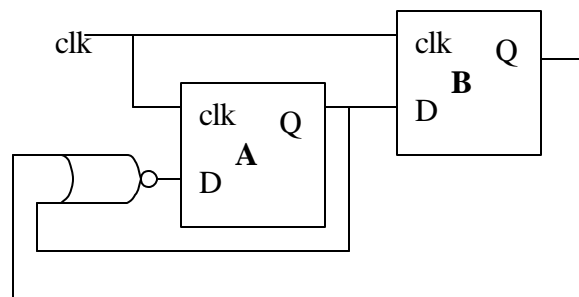


CLK	D	$Q_{n+1}$	$\bar{Q}_{n+1}$
	0	0	1
	1	1	0
	X	$Q_n$	$\bar{Q}_n$

- B. Test the truth table above using one of the data flip-flops on the IC.  
 C. Use both flip-flops to construct a count-by-four circuit (similar to problem 12-5 of the homework).  
 D. Use clock pulse at a frequency of 1 Hz as input to the count-by-four circuit. Connect the clock pulse to one of the indicators and the output of the circuit to another indicator. By carefully watching the lights, sketch the input (clock) and output waveforms.

**Questions:** In what sense does the circuit count by four? Is the circuit a synchronous counter or a ripple counter? Explain

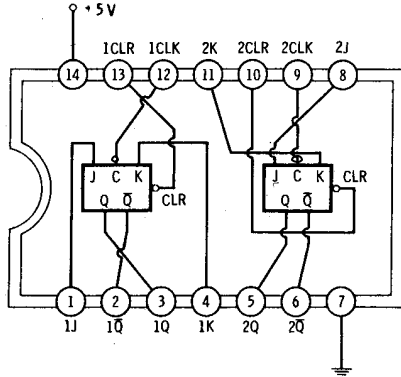
- E. Use the two data flip-flops and one of the NOR gates to make a count-by-three circuit. By carefully watching the lights, sketch the input (clock) and output waveforms.



**Questions:** Is the circuit that you made a synchronous counter or a ripple counter? Explain

### 8-3. JK Flip-Flops

- A. The 74LS107 is a TTL dual JK flip-flop with the connections shown below. Make the connections to ground and +5 V. Also, connect the clear (CLR) pins to +5 V for normal operation. When clear (also called reset) becomes high, the output is reset to the state  $Q=0$  and  $\bar{Q}=1$ . The truth table shows the behavior of a single JK flip-flop when clear is kept high. It indicates how the output changes when the clock input is low.



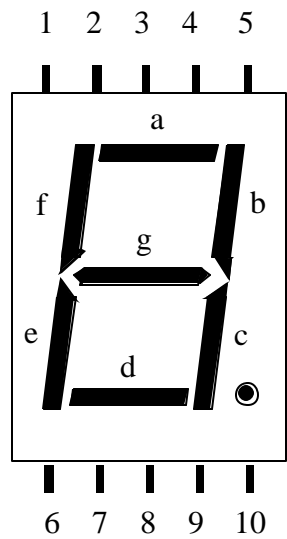
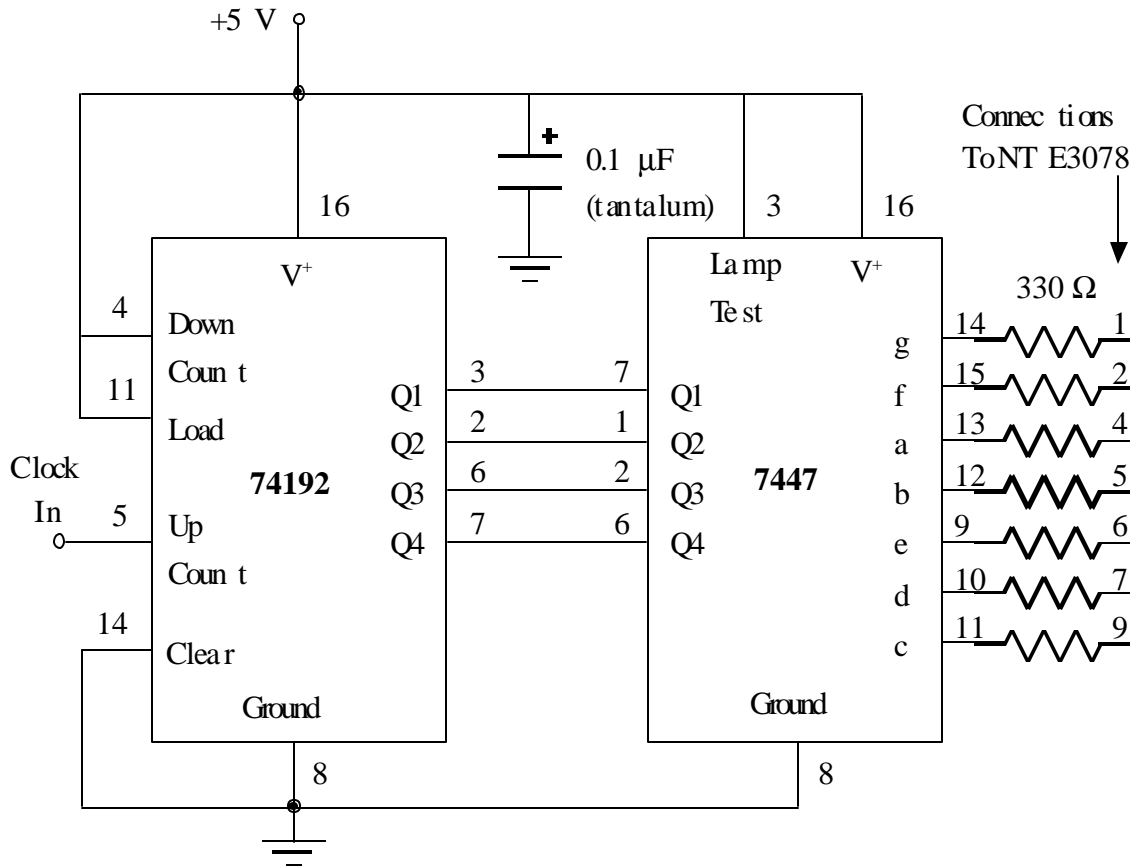
J	K	$Q_{n+1}$
0	0	$Q_n$
1	0	1
0	1	0
1	1	$\bar{Q}_n$

- B. Test the truth table above using one of the JK flip-flops on the 74LS107.  
 C. Use the JK flip-flops to construct a count-by-four circuit.  
 D. Use clock pulse at a frequency of 1 Hz as input to the count-by-four circuit. Connect the clock pulse to one of the indicators and the output of the circuit to another indicator. By carefully watching the lights, sketch the input (clock) and output waveforms.

**Question:** Is the circuit that you made a synchronous counter or a ripple counter? Explain

### 8-4. Decade Counter, Decoder, and Seven-Segment Display

- A. Wire up only the 74192 decade counter in the circuit below and connect the outputs to indicator lights. Use one of the switch outputs as a clock input to confirm that the outputs ( $Q_1$  to  $Q_4$ ) count up from zero to nine in BCD (binary-coded decimal).  
 B. Connect the 7447 BCD-to-seven-segment decoder to the NTE3078 seven-segment display (pins shown below) through 330- $\Omega$  resistors. Also, be sure to connect pin 3 of the display to +5 V. Pin 10 controls the decimal and there is no connection to pin 8. Input the clock signal set to a frequency of 1 Hz and observe the display.



**Question:** What happens when the connections for pin 4 and pin 5 of the decade counter are swapped?

**Question:** What happens when pin 14 (clear) of the decade counter is connected to one of the logic switch outputs? (What does the switch do?)